[10901/81]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

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| In re Application of: | Roman WOYZICHOVSKI |
| Serial No.: | 10/501,310 |
| Filed: | November 23, 2004 |
| For: | METHOD FOR INTERPOLATING AT LEAST TWO POSITION-DEPENDENT, PERIODIC ANALOG SIGNALS THAT ARE DEPHASED RELATIVE TO EACH OTHER |
| Examiner: | Jason Perilla |
| Art Unit: | 2611 |
| Confirmation No. | 6114 |

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Signature:/Julie Forero/

**REPLY BRIEF PURSUANT TO 37 C.F.R. § 41.41**

SIR:

This Reply Brief is filed in response to the Examiner's Answer dated August 18, 2009 in connection with the above-captioned application. For at least the reasons set forth below, as well as those set forth in the "Appeal Brief Pursuant to 37 C.F.R. § 41.37" ("the Appeal Brief") filed on April 29, 2009, it is respectfully submitted that the rejections contained in the Final Office Action dated September 5, 2008 should be reversed.

The Examiner's Answer recognizes at page 4 that "[i]n the combination of Liessner in view of Garverick, Liessner's embodiment must be converted to a purely digital

one." Furthermore, the Examiner's Answer contends at page 4 that "[o]ne skilled in the art would be . . . motivated to complete the conversion because of the advantages provided by digital implementations of analog devices." According to the Examiner's Answer, "proper digital implementations provide for zero loss in signal integrity as notoriously understood in the art." However, the analog-to-digital conversion process itself necessarily entails some degree of signal loss. Thus, the alleged motivation is based on underlying assumptions that are entirely flawed.

The Examiner's Answer further recognizes that the combination of Liessner and Garverick et al. as proposed in the Final Office Action would require modification of at least multipliers 12, 14, as well as adder 20, described by Liessner to change these components from analog form, as described by Liessner, into digital form. The Examiner's Answer then contends that the analog functions of detector 22, multi-step mode detector 23, async count generator 24, and up/down counter described by Liessner "could remain as they are presently configured" and that the output signal ES, in the proposed combination of Liessner and Garverick et al. "could remain as an analog signal." As best understood, the Examiner's Answer proposes a system in which sigma-delta modulators are provided in the system described by Liessner so that an analog-to-digital conversion of the analog input displacement signal is performed upstream of the multipliers 12, 14, in which the multipliers 12, 14 accept digital input signal (rather than analog input signals as described by Liessner) and output a digital signal (rather than an analog signal as described by Liessner) to adder 20, in which adder 20 accepts a digital input signal (rather than an analog signal as described by Liessner) and outputs an analog signal ES, and in which a digital signal Y is finally output by up/down counter 26. Such a modification would add significant complexity by requiring ***analog-to-digital*** conversion at the input of the system and a subsequent ***digital-to-analog*** conversion within the system at adder 20 so that error signal ES "could remain as an analog signal." This repeated conversion would necessarily introduce signal loss, thus negating the alleged motivation for making the proposed combination.

While the Examiner's Answer contends at page 11 that the alleged "principal advantage" of the combination of Liessner and Garverick et al. "would be to achieve zero loss in accuracy" and that "[o]ther advantages are commonly known to one having ordinary skill in the art and should likewise be considered," the Examiner's Answer fails in every respect to identify any such "other advantages." Moreover, and as indicated above, the

repeated conversion between digital and analog signals would ***introduce*** signal errors, *i.e.*, "zero loss in accuracy" would ***not*** be achieved by the proposed modification.

It should be noted that the Examiner's Answer takes two entirely contradictory positions regarding the level of redesign of Liessner that would be required. For example, the Examiner's Answer states on page 4 that "[i]n the combination of Liessner in view of Garverick, Liessner's embodiment must be converted to a purely digital one," whereas the Examiner's Answer states, in contradictory manner, on page 11 that:

> The Applicant notes that Liessner's output signal "ES" is an analog one. . . . The Examiner agrees and notes that, in the proposed combination, it could remain as an analog signal. That is, the analog functions of Liessner's circuit components 22, 23, 24, and 26 in figure 1 could remain as they are presently configured. Only Liessner's multipliers (12 and 14) and adder (20) would be modified to digital form for advantages of the combination to be achieved (i.e., the adder 20 could add digital values and output an analog signal in return).

Concerning the "specifiable time interval," as recited in claims 21 and 40 to 42, the Examiner's Answer reflects an apparent misapprehension of the underlying argument relating to these features. In this regard, Liessner specifies, for example, at col. 4, lines 39 to 43, that "the asynchronous count generator 24 operates without employing a clock signal." Without a clock signal or some other time-keeping mechanism, it is not apparent how Liessner could be considered to disclose, or even suggest, "accumulating ***over a specifiable time interval*** values of the string of results for generating the correctional values and the output signals" as recited in claim 20, "a filter configured to accumulate values of the string of results ***over a specified time interval*** to generate an address sequence to control the arithmetic unit to guide the string of results to satisfy the quality criterion as recited in claim 40, "accumulating over ***a specifiable time interval*** values of the combination output for generating the correctional values and output signals" as recited in claim 41, or "a filter configured to accumulate values of the combination output ***over a specified time interval*** to generate an address sequence to control the arithmetic unit to guide the string of results to satisfy the quality criterion." This is particularly acute considering the fact that Liessner specifically teaches away from the use of a clock signal. See, *e.g.*, col. 1, lines 51 to 68 and col. 4, lines 39 to 43. Indeed, the count generator is specified as a ***asynchronous count generator*** throughout the description by Liessner.

Thus, for at least foregoing reasons and those set forth in the Appeal Brief, it is respectfully submitted that the rejections set forth in the Final Office Action should be reversed.

Respectfully submitted,

Dated: October 14, 2009

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